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10/774,568	02/10/2004	Naoyuki Itakura	SON-2919	8508

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EXAMINER	
SHAPIRO, LEONID	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,568	ITAKURA ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16* is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *13-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Objections

Claim 13 is objected to because of the following informalities:

It is not clear what **ans** means?

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Asada et al. (US Patent No. 5,883,609).

As to claim 1, Asada et al. teaches a display device having at least a different resolution first mode and second mode having a lower resolution than said first mode (See Col. 1, Lines 7-15), comprising:

a pixel portion comprised of pixel circuits, for writing pixel data into pixel cells through switching elements, arranged so as to form a matrix of at least a plurality of rows (See Fig. 1, items i,j,101,TFT, Col. 3, Lines 17-45);

a plurality of scan lines arranged so as to correspond to a row arrangement of said pixel circuits and controlling conduction of said switching elements;

at least one signal line arranged so as to correspond to a column arrangement of said pixel circuits and propagating said pixel data (See Fig. 1, items i,j,101, Col. 3, Lines 17-45); and

a vertical drive circuit (in the reference is equivalent to Address Decoder 102) a vertical drive circuit including a plurality of switch circuits, each switch circuit coupling an adjacent plurality of scan lines in the row direction, the switch circuits adapting the vertical drive circuit to transmit scan pulses along scanning said scan lines in a row direction and successively select the pixel circuits connected to the scan lines units of rows (See Fig. 1, items i,j,102, Col. 3, Lines 17-45) and successively transmit scan pulses along adjacent pluralities scan of said scan lines in the row direction (See Fig. 6, Gp-1,..., GP-1024, Col. 15, Lines 18-22) and successively select the pixel circuits connected to said plurality of scan lines in units of the plurality of rows in said second mode (See Fig. 8, Gp-1-Gp-2,..., GP-1024, Col. 16, Lines 13-29).

As to claim 9, Asada et al. teaches a method of driving a display device including a pixel portion comprised of pixel circuits, for writing pixel data into pixel cells through switching elements, arranged so as to form a matrix of at least a plurality of rows (See Fig. 1, items i,j,101,TFT, Col. 3, Lines 17-45);and a plurality of scan lines arranged so as to correspond to a row arrangement of said pixel circuits and controlling conduction of said switching elements (See Fig. 1, items i,j,101, Col. 3, Lines 17-45), comprising using a plurality of switch circuits, each switch circuit coupling an adjacent plurality of scan lines in row direction to perform the steps of:

successively transmitting scan pulses along said scan lines in a row direction and successively selecting the pixel circuits connected to the scan lines in units of rows in a first mode having a predetermined resolution (See Fig. 1, items i,j,102, Col. 3, Lines 17-45) and

successively transmitting scan pulses along adjacent pluralities of said scan lines in the row direction (See Fig. 6, Gp-1,..., GP-1024, Col. 15, Lines 18-22) and successively selecting the pixel circuits connected to said plurality of scan lines in units of the plurality of rows in said second mode having a lower resolution than said first mode (See Fig. 8, Gp-1-Gp-2,..., GP-1024, Col. 16, Lines 13-29).

As to claims 3-4,7 Asada et teaches a horizontal drive circuit including a selector having selector switches for selecting the pixel data and supplying the same to said signal lines, said selector switches formed by connecting pluralities of switches in parallel to the corresponding signal lines, making said pluralities of switches conductive and outputting the selected pixel data to the signal lines through said pluralities of switches in said first mode, and making any switches among said pluralities of switches conductive and outputting the selected pixel data to the signal lines through said switches in said second mode (See Fig. 23, items 208-1,..., 208-1280, from Col. 30, Line 21 to Col. 31, Line 44).

As to claims 2,10 Asada et al. teaches a rear edge timing of the scan pulses for outputting the scan pulses to be output to a plurality of scan lines to be scanned

simultaneously in parallel to the scan lines of a previous stage earlier than the rear edge timing of the scan pulses to be output to the scan lines of the next stage in said second mode (See Fig. 24, SP-1,...,SP80, from Col. 31, Line 45 to Col. 32, Line 31).

As to claim 5, Asada et al. teaches a plurality of said signal lines (See Fig. 23, items DS-1,...,DS-1280) and a plurality of horizontal drive circuits dividing said plurality of signal lines into a plurality of groups and supplying pixel data to the signal lines corresponding to the divided groups (See Fig. 23, items 207-1,...,207-16, Col. 30, Lines 34-38).

As to claim 6, Asada et al. teaches a plurality of said signal lines (See Fig. 23, items DS-1,...,DS-1280) and a plurality of horizontal drive circuits dividing said plurality of signal lines into a plurality of groups and supplying pixel data to the signal lines corresponding to the divided groups (See Fig. 23, items 207-1,...,207-16, Col. 30, Lines 34-38),

each horizontal drive circuit including a selector having selector switches for selecting the pixel data and supplying the same to said signal lines, said selector switches formed by connecting pluralities of switches in parallel to the corresponding signal lines, making said pluralities of switches conductive and outputting the selected pixel data to the signal lines through said pluralities of switches in said first mode, and making any switches among said pluralities of switches conductive and outputting the selected pixel data to the signal lines through said switches in said second mode (See Fig. 23, items 208-1,..., 208-1280, from Col. 30, Line 21 to Col. 31, Line 44).

As to claims 8,11 Asada et al. teaches pixel cells are liquid crystal cells (See Col. 1, Lines 7-15).

As to claim 12 Asada et al. teaches each switch circuit couples adjacent scan lines in pairs of an odd scan line and even scan line (fig.5, item 12).

Response to Arguments

2. Applicant's arguments filed 10/15/07 have been fully considered but they are not persuasive:

On page 8, last paragraph and 1st paragraph on next page of Remark, Applicant's stated that Figs. 7 and 8 illustrate timing diagrams for a sample 256 scanline (P-1 - P-256) display, and show the differences between control signals for driving the LCD at both a high (1-fold) and low (2-foid) resolution, respectively. In both Figs. 7 and 8, the same number of control signals (8 pulse signals) are used to drive the same number of scan lines (2_8=256 scan lines). A comparison of the driving diagrams shows that, in the 2-fold resolution of Fig. 8, adjacent pairs of control signals (G-1 - G-8) are driven identically at periods twice as long as in the 1-fold resolution setting, disclosed in Fig. 7. These control signals do not provide the input nor effect the output of vertical drive circuit 12. Accordingly, Asada does not modify the operation of the vertical drive circuit 12 in order to obtain lower resolutions, instead accomplishing the desired result using identical, adjacent control signals (Fig. 23). However, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., accomplishing the desired

result using identical, adjacent control signals or do not provide the input nor effect the output of vertical drive circuit) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

On page 10, 2nd paragraph of Remark, Applicant's stated that **Asada does not teach or suggest using a single switch (or NAND gate) to control a** plurality **of scan lines.** Instead,, as illustrated in Figure 5 of Asada (provided above), Asada teaches that each NAND gate accepts an input control signal which operates the NAND gate independently. Furthermore, each NAND gate only affects a single scan line.

However, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **using a single switch (or NAND gate) to control a** plurality **of scan lines**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

On page 10, 3rd paragraph of Remark, Applicant's stated that each switch circuit coupling an adjacent plurality of scan lines. However, Asada et al. teaches each switch circuit coupling an adjacent plurality of scan lines (fig. 5, item 12).

Allowable Subject Matter

1. Claim 16 is allowed.

Relative to claim 16 the major difference between the teaching of the prior art of record (Asada et al.) and the instant invention is that a plurality of shirt registers; a plurality of sampling latches; and a plurality of power supply level shifters; each scan line in the vertical drive circuit being exclusive associated with corresponding shift register, a corresponding sampling latch and a corresponding power supply level shifter, and the output of each shift register corresponding a scan line is input to a switch circuit, the switch circuit having an input corresponding with each scan line and an output corresponding to each scan line, and the outputs from the switch circuit corresponding to each scan line inputs data to the sampling latches corresponding to each scan line.

2. Claims 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 13 the major difference between the teaching of the prior art of record (Asada et al.) and the instant invention is that each switch circuit include input for the adjacent scan lines and at least one mode signal.

Relative to claim 14 the major difference between the teaching of the prior art of

record (Asada et al.) and the instant invention is that the display device is in the first mode, the plurality of switches switch do not effect the scan pulses output by the vertical drive circuit, and when the display device is in the second mode plurality of switches combines the scan pulses of the coupled scan lines and outputs the combined scan pulses along the adjacent plurality of scan lines.

Relative to claim 15 the major difference between the teaching of the prior art of record (Asada et al.) and the instant invention is that the at least one mode signal comprises at least one non-pulsing signal representing whether the display device is operating in the first mode or second mode.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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